REMARKS

Claims 3, 5-16, 18, and 21-22 are pending in the application. Claims 5, 6, 8, 9, 11, 15, 18, 21, and 22 are rejected. Claims 7 and 10 are objected to. Claims 3, 12-14, and 16 are allowed. In view of the following remarks, reconsideration of the application is respectfully requested.

Response to 35 U.S.C. § 102 Claim Rejections

Claims 5 and 15 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,810,031 ("Hegde"). Applicant respectfully traverses this rejection, and submits that Hegde fails to teach each element of either claim, and therefore does not anticipate claims 5 and 15.

The rejection states, in part, that Hegde teaches a data rate controller comprising "a bandwidth tracker to identify an allocated bandwidth and to prevent the input port from connecting to the output port when the bandwidth is used up (col. 7, line 66 through col. 8, line 5.)" (Office Action at 2, numbered paragraph 1.) This Hegde reference fails to disclose a bandwidth tracker that prevents an input port from connecting to an output port when bandwidth is used up (claim 5), and a method that prevents input ports from sending requests for the input ports when the bandwidth allocated to the input ports has been exhausted (claim 15), as claimed. Hegde never exhausts bandwidth and therefore never discloses preventing connections and requests. Hegde discloses that "the PPU 106 of the IPE card 104 calculates the bandwidth request information for each data flow based on the corresponding buffer occupancy for each data flow." (Hegde, col. 9, ll. 5-7) "The bandwidth request for each data flow is then determined as follows:" Bandwidth Request = DDR+ABO, where DDR is a draw-down request and ABO is accumulated buffer occupancy. (*Id.*, ll. 19-30) The MPPUs merely aggregate the requests from each PPU. (*Id.*, ll. 38-41) Accordingly, Hegde's Credit and draw-down cannot function as the claimed controller and method, at least because it can never prevent the card from requesting (and receiving) bandwidth based on Accumulated Buffer Occupancy, no matter what actual bandwidth the card has been using. Hegde, and in particular the section of Hegde included in the rejection for support, fail to show this limitation. The paragraphs at column 7, lines 1-27 further explain how Hegde fairly divides available bandwidth, but never prevents requests or port connections (lines 18-23 even indicate the possibility of input ports overwhelming the switch fabric, causing packet drops in the switch fabric).

Based at least on the differences identified above, Applicant respectfully submits that Hegde cannot anticipate claims 5 and 15.

Response to 35 U.S.C. § 103 Claim Rejections

Claims 6, 8-9, 11, 18, and 21-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hegde in view of U.S. Patent No. 6,449,283 ("Chao"). Applicant respectfully traverses this rejection, and submits that the combination of Hegde and Chao fails to present a *prima facie* case of obviousness for any rejected claim.

As a first matter, Chao teaches nothing that overcomes the deficiencies pointed out above in Hegde. As similar claim limitations to those of claims 5 and 15 exist in each of claims 6, 8-9, 11, 18, and 21-22, for this reason alone the combination of references fails to teach all elements of any rejected claim, and therefore a *prima facie* case of obviousness is lacking.

Furthermore, Applicant respectfully disagrees with the assertion that Chao discloses multiple rate controllers assigned to each input-output port combination. The identified section and figure of Chao show multiple arbiters, not multiple rate controllers. The arbiters merely operate in round-robin fashion and make no attempt to limit rate. For instance, if at input 1 (Figure 11) traffic was waiting only in VOQ 1, it is clear that Chao would repeatedly request transmission from input 1 to output 1, no matter what the resulting rate. Thus Chao does not teach or suggest that each input port-output port combination should have a data rate controller with the limitations of claim 6, or that data rate controllers should prevent input ports that have exceeded a data rate limit from sending connection requests to the scheduler. Accordingly, the prior art fails to teach or suggest all elements of these claims, and fails to provide a motivation for combining the references as suggested by the Examiner.

Regarding claim 9, the cited section of Chao also does not disclose selecting input ports based on weight of packets. The cited section discloses sending multiple requests, one for each VOQ with data pending, but does not mention weighting the requests based on weight of packets. The described embodiment uses "request bits" that have no way of conveying such information, even if it was desired. (Chao, col. 17, ll. 1-48)

Finally, regarding claim 22, Applicant disagrees with the assertion that Chao's output arbiters are data rate controllers that control a rate that data is received by the output ports from multiple input ports. Like with Chao's input arbiters, the output arbiters merely operate in round-robin fashion and make no attempt to limit a rate.

Accordingly, Applicant respectfully submits that the combination of Chao and Hegde fails to teach or suggest the invention as claimed, or even all elements of the invention, and thus a *prima facie* case of obviousness is lacking.

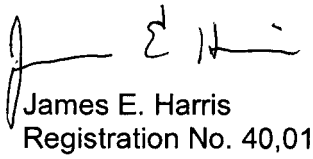
Response to Claim Objections

Claims 7 and 10 were objected to as being dependent upon a rejected base claim, but were found otherwise allowable. In view of the arguments presented above for the patentability of the base claim, Applicant has chosen not to amend these claims.

Conclusion

Applicant respectfully requests that the application be allowed in present form.

Respectfully submitted,



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